THE SIMULATED POWER CONDITIONER FOR PV SYSTEMS BY ELECTRONIC DEVICES FOR THE ULTRA SCALED-DOWN NETWORK SIMULATOR

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ABSTRACT: PV systems have spread rapidly around distribution network. In case of a large number of PV systems are connected to the distribution network, safety issue by islanding and degradation of power quality which is caused by the over voltage and the harmonic can be happened. Therefore, it is necessary to evaluate PV system at the condition which a large number of PV systems are connected to the distribution network. The ultra scaled-down network simulator which emulated the distribution network by electric devices was developed to evaluate the condition. It has some advantages in comparison to full-scale network simulator, the scaled-down network simulator and simulation using personal computer. Consequently, this paper proposes a simulated power conditioning system (PCS) for PV system which is composed of electronic devices to test cheaply a PCS at the condition by using the ultra scaled-down network simulator on small space. Field Programmable Gate Array (FPGA) is used to design functions flexibly in control system of the simulated PCS. The required functions of the simulated PCS are functions which general PCSs equip for grid-connection. In this paper, synchronize control, constant current control, over volatege relay and under voltage relay in functions which will be equiped are reported.
Keywords: Grid Connected, PV system, Power Conditioning

1 INTRODUCTION

Dispersed Generators (DGs) for grid-connection has spread rapidly. In case of a large number of DGs are connected to the distribution network, safety issue by islanding and degradation of power quality by the over voltage and the harmonic can be happen. Therefore, it is necessary to evaluate DGs in the condition which a large number of DGs are connected to the network.

There is a full-scale network simulator for testing such a condition directly. However, it is very expensive and needs large space. Therefore, a scaled-down network simulator was developed [1]. It makes a full-scale grid downscale, but it still needs large space. In others assessment methods, digital simulation methods by a personal computer have advantages in size of test equipment, cost and usability. However, long time is required to obtain a solution under a complex network. Moreover, it's difficult to simulate the real performance of DGs. On the other hand, assessment methods employing analog circuits can obtain a real-time result from experiments in a timely manner. To evaluate a complex network including actual DGs is an advantage of these methods.

Consequently, the ultra scaled-down network simulator was developed at laboratory as an analog simulator [2]. This simulator has advantages in size, cost and extensibility for adapting to the condition which a large number of DGs are connected. It is composed of electronic circuits include Active Power Interface (API) [3]. By using the API, an actual DG and this simulator can be connected in the equivalent per API. However, connecting a large number of actual DGs to this simulator is difficult because of cost to purchase a large number of DGs and large space for installing a large number of APIs. If a downscaled DG is developed as an electronic circuit, it is possible to simulate condition which a large number of DGs are connected to the network in small power level.

In this study, actual DGs are emulated by electronic devices. Functions of the simulated DG have to be the same of general DGs. In addition, if functions of the simulated DG are user-selectable, large variety of DGs connecting to the network can be emulated. The simulated DG can perform the various types of actual DGs by using FPGA. In this paper, the simulated PCS for PV systems which is composed of electronic devices for the ultra scaled-down network simulator is proposed.

2 REQUIRED SPECIFICATION OF THE SIMULATED PCS

Requisitions of the simulated PCS are shown below.

- To equip same functions and control which general PCSs equip for grid-connection.
- Functions and parameters for control are selectable.
- Small size
- Connectable to the ultra scaled-down network simulator
- Output of the simulated PCS is ideal sine waveform with no switching noise.

The last requisition is a requisition as test equipment. In the case of it evaluates an actual PCS in the condition which a large number of PCSs are connected to the distribution network by using a large number of the simulated PCS, operation of an actual PCS is clear if the output of the simulated PCS is ideal sine waveform with no switching noise.

FPGA is used in control system of the simulated PCS to suit as requisitions above. FPGA has an ability of parallel processing. Therefore, some functions which control frequency is different can be installed in a chip of FPGA and the simulated PCS becomes small size. And also, functions of the simulated PCS are designed flexibly because internal logic of FPGA is customizable by rewriting Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). Table I shows specification of the simulated PCS. Rated output power, rated output voltage, rated output current and frequency are designed to connect the simulated PCS

to the ultra scaled-down network simulator. Methods of grid protection, other functions and control which general PCSs equip are shown in Table I. In this paper, synchronize control, constant current control and OFR/UFR are reported.

Table I: Required specification of the simulated PCS

Rated output power	0.1 [W]
Rated output voltage	5/10 [V]
Rated output current	20 [mA]
Frequency	50/60 [Hz]
Grid protection	• OVR/UVR*1 • OFR/UFR*2 • Islanding detecting function (Active + passive)
Others function and control	• Start-and-stop control • Synchronize control • Power factor control • Constant current control • Over voltage protection

*1: OVR/UVR: Over Voltage Relay/ Under Voltage Relay
*2: OFR/UFR: Over Frequency Relay/ Under Frequency Relay

3 Architecture of the simulated PCS

3.1 Circuit design

The simulated PCS circuit is shown in Fig. 1. The simulated PCS circuit can be divided into four parts. The four parts are phase detection, FPGA, D/A converter and current sensor. A signal of grid phase is created, in the part of phase detection which is composed of a comparator (NJM2903, JRC). It is used to calculate the grid frequency in the FPGA (Cyclone EP1C6T144C8, Altera). The signal of grid phase is 1 bit. This signal is high during positive periods of the grid voltage, and this signal is low during negative periods of the grid voltage. In the FPGA, some control processing are operated. For example, synchronize control, constant current control and OFR/UFR and so on. The definitive output of the FPGA is 8 bit digital data of sine-wave. By inputting the digital data into the D/A converter (DAC0800, National Semiconductor), the digital data are converted analog sine-wave. The D/A converter has two output pins, and the relationship between these pins is inversion. Therefore, a differential amplifier has to be connected the D/A converter for getting desired waveform. The output of differential amplifier is an output of the simulated PCS. Shunt resistance R_S is connected for sensing output current. Voltage of R_S, V_S is converted into 8 bit digital data by the A/D converter (AD7821, Analog Devices) as output current of the simulated PCS. The converted data are used to operate constant current control in the FPGA.

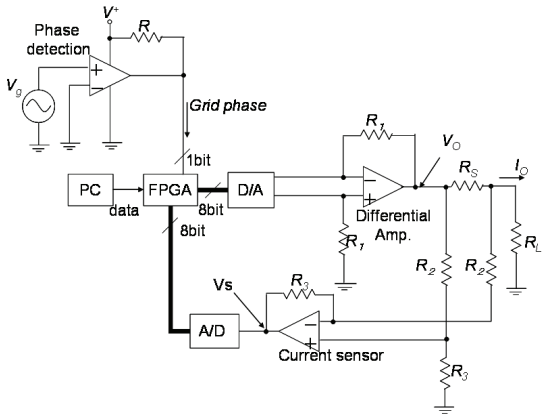

Figure 1: The simulated PCS circuit

3.2 Internal logic of FPGA

The internal logic is shown in Fig. 2. Each blocks are explained below.

3.2.1 Digital PLL

The signal of grid phase which is made at phase detection is input into frequency counter. Internal clocks of the FPGA are counted during grid phase is high in frequency counter. For example, if internal clock is 100[kHz] and frequency of grid phase is 50[Hz] (duty ratio is 0.5), number of internal clock is 1020. The grid frequency is calculated in this way.

Output frequency of Numerical Controlled Oscillator (NCO) is changed by input value which is calculated at frequency counter. For example, output frequency of NCO is 10[kHz] when input value is 1020, and output frequency of NCO is 20[kHz] when input value is 510. Together with frequency counter and NCO are called Digital Phase Locked Loop (PLL).

3.2.2 Sine data

In sine data, sine-wave data which are 200 points are stored. The data are output one by one. The output frequency is the same frequency which is the input frequency. For example, the sine-wave data is output one by one per 100[us] when input frequency is 10[kHz]. Overview of sine-wave is 50[Hz] when all 200 points data finish to output. Therefore, output frequency of the simulated PCS is 50[Hz] when grid frequency is 50[Hz]. The synchronize control is controlled as above processing.

3.2.3 Constant current control

An algorism of constant current control is one of PI control. Target value of constant current control is output from sine data and return value is *Vs*. Formulas of PI control are shown below. Error of control system, *E(n)* is shown in formula (1) using target value is *R(n)* and return value is *X(n)*. n means n^{th} discrete-valued data.

$$E(n) = R(n) - X(n) \qquad (1)$$

If previous output of PI control *U(n-1)* and previous error *E(n-1)* are stored, output of PI control *U(n)* can be calculated by twice of multiplication and adder-subtractor. If proportional gain is K_P and integral gain is K_i, *U(n-1)* is shown in formula (2) below. *U(n)* is input into the D/A converter.

$$U(n) = K_P E(n) + K_i \sum_{i=1}^{n} E(i) \qquad (2)$$
$$= U(n-1) + (K_P + K_i)E(n) - K_P E(n-1)$$

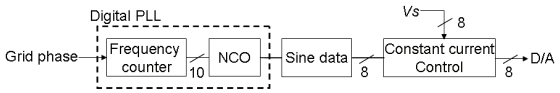

Figure 2: Internal logic of the FPGA

3.2.4 OFR/UFR

3.2.4.1 Algorism

The block diagram of OFR/UFR is shown in Fig. 3. The grid frequency is calculated in the same way of section 3.2.1 in frequency counter. The result of frequency counter is processed in moving average for avoiding detecting transient fluctuation of the grid frequency. An equation of moving average is shown in formula (3) below. C_n means n^{th} data and N means number of data.

$$Average_n = \frac{C_n + C_{n+1} + \cdots + C_{n+N-1}}{N} \qquad (3)$$

In the case of detecting over or under frequency, a signal which stops the simulated PCS is output from determination of OF/ UF in 1[s].

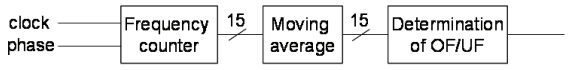

Figure 3: The block diagram of OFR/UFR

3.3.4.2 Thresholds of over frequency and under frequency [4]

Grid-interconnection code which shows technical requirements for grid connection has been published to help to spread DGs in Japan. About thresholds of OFR and UFR are shown in grid-interconnection code. Table II shows the thresholds. In this paper, a threshold at over voltage is 51[Hz] and a threshold at under voltage is 49[Hz] are configured based on grid-interconnection code.

Table II: Standard thresholds for OFR/ UFR

	Level of detection	Detecting time
OFR	51.0 Hz [50.5~51.5 Hz]	1 s [0.5~2 s]
UFR	48.5Hz [48.5~49.5 Hz]	1 s [0.5~2 s]

4 EXPERIMENT OF THE SIMULATED PCS

4.1 Synchronize control and constant current control

Table III shows system parameters in the simulated PCS circuit. R_2 and R_3 are settled on such value in Table III because E(n) needs to be zero when output current is 20[mA]. In other words, *Vs* is about 2.9[V] and E(n) is zero when target value is settled on 20[mA]. Observed waveforms are shown in Fig. 4. From the upper waveform in Fig.4, V_g shows the grid voltage, *grid phase* which made at phase detection in Fig.1, *Vo* shows the output voltage of the simulated PCS and *Vs* shows the output voltage at a part of the current sensor and it shows the output current of the simulated PCS. According to Fig. 4, V_S was synchronized with the grid voltage V_g and a value of V_S was almost 2.9[V] of target value. Therefore, it found that synchronize control and constant current control were operated.

Table III: System parameters in the simulated PCS circuit

R	10 [kΩ]
R_1	5 [kΩ]
R_2	1 [kΩ]
R_3	147 [kΩ]
R_S	1 [Ω]
R_L	300 [Ω]

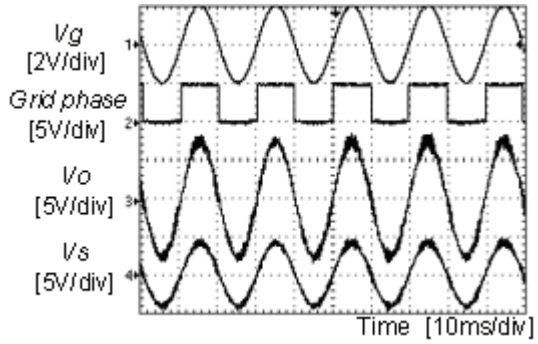

Figure 4: Observed waveforms of the simulated PCS

4.2 OFR/UFR

In this experiment, the part of phase detection in Fig. 1 is removed because the grid phase which has 3 change patterns is created in the FPGA. First, the grid phase is changed from 45[Hz] to 55[Hz] by 0.1[Hz]. Second, the grid phase is changed from 50[Hz] to 52[Hz] steeply. Third, the grid phase is changed from 50[Hz] to 48[Hz] steeply. And, N in formula (3) is configured at 16 in this experiment. Each results of changed grid phase are shown in Fig. 5, 6 and 7. From the upper waveform in Fig. 5, 6 and 7 each, *grid phase* which is created in the FPGA, *S* shows whether *grid phase* is in 49 ~ 51[Hz], V_S shows the output of the simulated PCS in the same way of section 4.1. In the case of *S* is high, *grid phase* is in 49 ~ 51[Hz], in the case of *S* is low, *grid phase* isn't in 49 ~ 51[Hz].

According to Fig. 5, the simulated PCS stopped after detecting over frequency in 1.079[s]. Similarly, the simulated PCS stopped in 0.952[s] in Fig. 6 and in 0.950[s] in Fig. 7. In these experiments, the simulated PCS stopped in around 1[s] when over frequency or under frequency were detected.

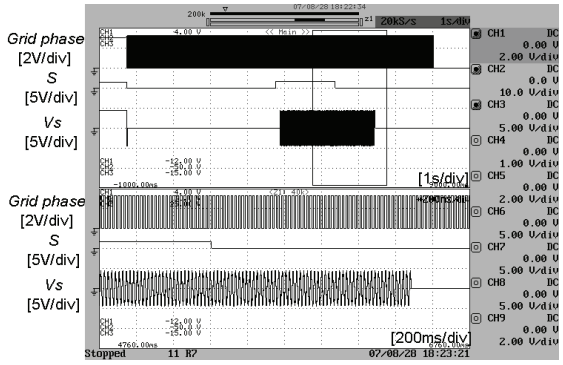

Figure 5: Observed waveforms at the experiment of the grid phase changes from 45[Hz] to 55[Hz] by 0.1[Hz]

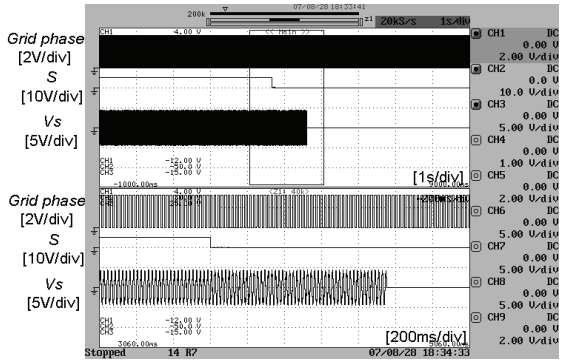

Figure 6: Observed waveforms at the experiment of the grid phase changes from 50[Hz] to 52[Hz] steeply

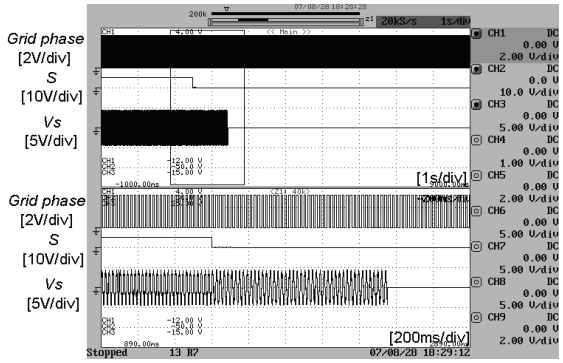

Figure 7: Observed waveforms at the experiment of the grid phase changes from 50[Hz] to 48[Hz] steeply

5 CONCLUSION

This paper has proposed the simulated PCS which is composed of electronic devices. It has functions for grid-connection which general PCSs equip and is connectable to the ultra scaled-down network simulator. By using FPGA in control system, functions of the simulated PCS are designed flexibly. The presented simulated PCS has equipped synchronize control, constant current control and OFR/UFR. By experiments, it found these controls and function were operated properly.

For the future, the simulated PCS will equip the others function and control in Table I. And then, the simulated PCS will be connected to the ultra scaled-down network simulator for test of grid-connection.

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